What is claimed is:

1. A power-rail ESD protection circuit with a dual trigger design, which is coupled between a first power line and a second power line connected to an IC device for protecting the IC device against ESD on the first power line and the second power line;

the power-rail ESD protection circuit comprising:

a control circuit, which is coupled between the first power line and the second power line, and which is capable of, in the event of ESD in the first power line and the second power line, being triggered by the ESD to output a substrate-triggering voltage and a gate-driving voltage; and

a MOS device, whose source and drain are respectively connected to the first power line and the second power line, whose substrate is coupled to receive the substrate-triggering voltage, and whose gate is coupled to receive the gate-driving voltage, for bypassing ESD current from the first power line and the second power line.

2. The power-rail ESD protection circuit of claim 1, wherein the MOS device is an NMOS device.

3. The power-rail ESD protection circuit of claim 2, wherein the control circuit includes *N* serially-cascaded diodes, wherein the positive end of the first diode is connected to the first power line and the negative end of the last diode is connected to the second power line, and wherein the positive end of the (*A*)th diode is connected to the substrate of the NMOS device, and the positive end of the (*B*)th diode is connected to the gate of the NMOS device, where *A* and *B* are predetermined to allow the positive end of the (*A*)th diode to supply the substrate-triggering voltage and the positive end of the (*B*)th diode to supply the gate-driving voltage;

and wherein in the event of ESD in the first power line and the second power line, and the substrate-triggering voltage applied to the substrate of the NMOS device is greater than the gate-driving voltage applied to the gate of the NMOS device.

4. The power-rail ESD protection circuit of claim 3, wherein the *N* serially-cascaded diodes are implemented by *N* NMOS devices, each NMOS device having its drain and gate tied together and its source and substrate tied together.

5. The power-rail ESD protection circuit of claim 2, wherein the control circuit includes:

a resistor having a first end and a second end, wherein the first end is connected to the first power line;

a capacitor having a first end and a second end, wherein the first end is connected to the second end of the resistor, while the second end is connected to the second power line; and

an inverter having a first power port connected to the first power line, a second power port connected to the second power line, an input port connected to the second end of the resistor, and an output port connected to both the gate and the substrate of the NMOS device;

wherein in the event of ESD in the first power line and the second power line, the substrate-triggering voltage applied to the substrate of the NMOS device is equal to the gate-driving voltage applied to the gate of the NMOS device.

6. The power-rail ESD protection circuit of claim 2, wherein the control circuit includes *N* serially-cascaded diodes, wherein the positive end of the first diode is connected to the first power line and the negative end of the last diode is connected to the second power line, and wherein the positive end of the (*A*)th diode is connected to the substrate of the NMOS device,

and the positive end of the (*B*)th diode is connected to the gate of the NMOS device, where *A* and *B* are predetermined to allow the positive end of the (*A*)th diode to supply the substrate-triggering voltage and the positive end of the (*B*)th diode to supply the gate-driving voltage, and the substrate-triggering voltage applied to the substrate of the NMOS device is smaller than the gate-driving voltage applied to the gate of the NMOS device.

7. The power-rail ESD protection circuit of claim 6, wherein the *N* serially-cascaded diodes are implemented by *N* NMOS devices, each NMOS device having its drain and gate tied together and its source and substrate tied together. The *N* serially-cascaded diodes are implemented by *N* PMOS devices, each PMOS device having its drain and gate tied together and its source and substrate tied together.

8. The power-rail ESD protection circuit of claim 1, wherein the MOS device is a PMOS device.

9. The power-rail ESD protection circuit of claim 8, wherein the control circuit includes:

a resistor having a first end and a second end, wherein the first end is connected to the first power line;

a capacitor having a first end and a second end, wherein the first end is connected to the second end of the resistor, while the second end is connected to the second power line;

a first inverter having a first power port, a second power port, an input port, and an output port; wherein the first power port is connected to the first power line, the second power port is connected to the second power line, and the input port is connected to the second end of the resistor;

a second inverter having a first power port, a second power port, an input port, and an output port; wherein the first power port is connected to the first power line, the input port is connected to the output port of the first inverter, and the output port is connected to the substrate of the PMOS device; and

a plurality of serially-cascaded diodes, wherein the first diode has its positive end connected to the second power line of the second inverter, and the last diode has its negative end connected to the second power line, and wherein one of the diodes has its positive end connected to the gate of the PMOS device;

wherein In the event of ESD in the first power line and the second power line, the substrate-triggering voltage applied to the substrate of the PMOS device is greater than the gate-driving voltage applied to the gate of the PMOS device.

10. The power-rail ESD protection circuit of claim 8, wherein the control circuit includes:

a resistor having a first end and a second end, wherein the first end is connected to the first power line;

a capacitor having a first end and a second end, wherein the first end is connected to the second end of the resistor, while the second end is connected to the second power line;

a first inverter having a first power port, a second power port, an input port, and an output port; wherein the first power port is connected to the first power line, the second power port is connected to the second power line, and the input port is connected to the second end of the resistor; and

a second inverter having a first power port, a second power port, an input port, and an output port; wherein the first power port is connected to the first power line, the second power

port is connected to the second power line. the input port is connected to the output port of the first inverter. and the output port is connected to both the substrate and the gate of the PMOS device;

wherein In the event of ESD in the first power line and the second power line, the substrate-triggering voltage applied to the substrate of the PMOS device is equal to the gate-driving voltage applied to the gate of the PMOS device.

11. The power-rail ESD protection circuit of claim 8, wherein the control circuit includes *N* serially-cascaded diodes, wherein the positive end of the first diode is connected to the first power line and the negative end of the last diode is connected to the second power line, wherein the positive end of the (*A*)th diode is connected to the substrate of the PMOS device, and the positive end of the (*B*)th diode is connected to the gate of the PMOS, where *A* and *B* are predetermined to allow the positive end of the (*A*)th diode to supply the substrate-triggering voltage and the positive end of the (*B*)th diode to supply the gate-driving voltage; and wherein in the event of ESD in the first power line and the second power line, and the substrate-triggering voltage applied to the substrate of the PMOS device is smaller than the gate-driving voltage applied to the gate of the PMOS device.

12. The power-rail ESD protection circuit of claim 11, wherein the *N* serially-cascaded diodes are implemented by *N* NMOS devices, each NMOS device having its drain and gate tied together and its source and substrate tied together.

13. A power-rail electrostatic discharge protection circuit with a dual trigger design, which is coupled between a first power line and a second power line connected to an IC device for protecting the IC device against ESD on the first power line and the second power line;

the power-rail ESD protection circuit comprising:

a control circuit, which is coupled between the first power line and the second power line, and which is capable of, in the event of ESD in the first power line and the second power line, being triggered by the ESD to output a substrate-triggering voltage and a gate-driving voltage;

an NMOS device, whose source and drain are respectively connected to the first power line and the second power line, whose substrate and gate are connected together to receive the substrate-triggering voltage from the control circuit;

a PMOS device, whose source and drain are respectively connected to the first power line and the second power line, whose substrate and gate are connected together to receive the substrate-triggering voltage from the control circuit;

14. The power-rail ESD protection circuit of claim 13, wherein the control circuit includes:

a resistor having a first end and a second end, wherein the first end is connected to the first power line;

a capacitor having a first end and a second end, wherein the first end is connected to the second end of the resistor, while the second end is connected to the second power line;

a first inverter having a first power port, a second power port, an input port, and an output port; wherein the first power port is connected to the first power line, the second power port is connected to the second power line, the input port is connected to the second end of the resistor, and the output port is connected to both the substrate and gate of the NMOS device; and

a second inverter having a first power port, a second power port, an input port, and an output port; wherein the first power port is connected to the first power line, the second power port is connected to the second power line, the input port is connected to the output port of the first inverter, and the output port is connected to both the substrate and the gate of the PMOS device;

wherein in the event of ESD in the first power line and the second power line, the substrate-triggering voltage applied to the substrate of the NMOS device is equal to the gate-driving voltage applied to the gate of the NMOS device, and the substrate-triggering voltage applied to the substrate of the PMOS device is equal to the gate-driving voltage applied to the gate of the PMOS device.